**IN THE CLAIMS:**

Claims 1, 3-13, and 15-16 are pending in the current application. No claims have been amended, canceled, or added. A complete list of the pending claims is presented below for the Examiner's convenience:

1. (Previously presented) A system, comprising:

a bus including a power line;

a bus bridge device including an internal logic unit; and

a power regulator to deliver power to the power line, the power regulator further to assert a fault signal to the bus bridge device if a power fault is detected the bus bridge device to disconnect the internal logic unit from the bus in response to an assertion of the fault signal.

2. Cancelled

3. (Previously presented) The system of claim 1, the power regulator to cease to deliver power to the power line if a power fault is detected.

4. (Original) The system of claim 3, the bus bridge device to assert an interrupt signal in response to the assertion of the fault signal.

5. (Original) The system of claim 3, the bus bridge device to assert an error signal in response to the assertion of the fault signal.

6. (Original) The system of claim 3, the bus bridge device to assert a power enable signal to the power regulator upon system startup, the power regulator to deliver power to the power line in response to the assertion of the power enable signal.

7. (Original) The system of claim 6, the bus bridge device to deassert the power enable signal follow the assertion of the fault signal.

8. (Original) The system of claim 7, the power regulator module to deassert the fault signal in response to the deassertion of the power enable signal.

9. (Original) The system of claim 8, wherein the bus is a PCI bus.

10. (Original) A bus bridge device, comprising:

a bus interface unit to coupled to bus bridge device to a bus;

an internal logic unit coupled to the bus interface unit; and

a fault signal input, the bus bridge device to disconnect the internal logic unit from the bus in response to an assertion of the fault signal.

11. (Original) The bus bridge device of claim 10, further comprising an interrupt signal output, the bus bridge device to assert the interrupt signal output in response to the assertion of the fault signal.

12. (Original) The bus bridge device of claim 10, further comprising an error signal output, the bus bridge device to assert the error signal in response to the assertion of the fault signal.

13. (Previously presented) A method, comprising:

applying power to a bus;

detecting a power fault;

removing power from the bus; and

asserting a fault signal to a bus bridge device; and

disconnecting an internal logic unit within the bus bridge device from the bus in response to the assertion of the fault signal.

14. Cancelled

15. (Previously presented) The method of claim 13, further comprising asserting an interrupt signal in response to the assertion of the fault signal.

16. (Previously presented) The method of claim 13, further comprising asserting an error signal in response to the assertion of the fault signal.